CLAIMS

What is claimed is:

1. A logic board designed for circuit emulation, comprising

a plurality of input/output (I/O) pins;

a plurality of emulation integrated circuits (IC), each having reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of a partition of an IC design; and

a plurality of on-board data processing resources coupled to said emulation ICs to locally retrieve from said emulation ICs state data of emulation state circuit elements, responsive to a monitor and report request received through said I/O pins, and to locally analyze the retrieved state data to detect occurrence of one or more events, as well as report on the occurrence of the one or more events upon their detection through said I/O pins.

2. The logic board as set forth in claim 1, wherein the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board to perform said responsive local retrieval of state data of the emulation state circuit elements, local analysis of the retrieved state data, and reporting of event detection, and a processor coupled to the storage medium to execute the programming instructions.

3. The logic board as set forth in claim 1, wherein at least one of said emulation ICs comprises on-chip data processing resources to cooperate and assist said on-

board data processing resources to perform said local monitoring and reporting of monitored events.

4. The logic board as set forth in claim 1, wherein the on-board data processing resources are further employed to locally generate a plurality of testing stimuli, and locally apply said locally generated testing stimuli to the partition of the IC design being emulated, responsive to a testing request received through said I/O pins.

5. The logic board as set forth in claim 4, wherein the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board to perform said responsive local generation and application of stimuli, and a processor coupled to the storage medium to execute the programming instructions.

6. The logic board as set forth in claim 4, wherein at least one of said emulation ICs comprises on-chip data processing resources to cooperate and assist said on-board data processing resources to perform said local generation and application of testing stimuli.

7. In an emulation apparatus, a method of operation comprising:

receiving by an emulation logic board, through input/output (I/O) pins of said logic board, a monitor and report request;

in response, locally retrieving from emulation ICs of said logic board state data of emulation state circuit elements of a partition of an IC design being emulated;

locally analyzing said retrieved state data to detect occurrence of one or more events; and

reporting through said I/O pins of said logic board occurrence of said one or more events, upon detection of their occurrence.

8. The method as set forth in claim 7, wherein at least some of said analysis and detection are performed by on-chip data processing resources of said emulation ICs, in lieu of retrieving the state data from the emulation ICs and then analyzing the state data to detect for the one or more events.

9. The method as set forth in claim 7, wherein the method further comprises locally generating on said logic board a plurality of testing stimuli, and applying said locally generated testing stimuli to the partition of the IC design being emulated, responsive to an external testing request received by said logic board through said I/O pins of the logic board.

10. The method as set forth in claim 9, wherein at least some of said generation of testing stimuli are performed by on-chip data processing resources of said emulation ICs instead.

11. A logic board designed for circuit emulation, comprising

a plurality of input/output (I/O) pins;

a plurality of emulation integrated circuits (IC), each having reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of a partition of an IC design; and

a plurality of on-board data processing resources coupled to said emulation ICs to locally generate a plurality of testing stimuli, and locally apply said locally generated testing stimuli to emulation circuit elements of said partition of the IC design being emulated, responsive to an external testing request received through said I/O pins.

12. The logic board as set forth in claim 11, wherein the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board to perform said responsive local generation and application of stimuli, and a processor coupled to the storage medium to execute the programming instructions.

13. The logic board as set forth in claim 12, wherein at least one of said emulation ICs comprises on-chip data processing resources to cooperate and assist said on-board data processing resources to perform said local generation and application of testing stimuli.

14. In an emulation apparatus, a method of operation comprising:

receiving by a logic board, through input/output (I/O) pins of said logic board, a testing request;

in response, locally generating on said logic board a plurality testing stimuli; and

locally applying said locally generated testing stimuli to emulation circuit elements of a partition of an IC design being emulated.

15. The method as set forth in claim 14, wherein at least some of said generation of testing stimuli are performed by on-chip data processing resources of said emulation ICs instead.

16. An emulation system comprising:

a plurality of logic boards, each having a plurality of emulation integrated circuits (IC) including reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of partitions of an IC design, and on-board data processing resources to locally and correspondingly retrieving state data of emulation state circuit elements from the emulation ICs, responsive monitor and report requests received through input/output (I/O) pins of the logic boards, and retrieving state data of the emulation state circuit elements from the emulation ICs, locally and correspondingly analyzing the retrieved state data for one or more events, and reporting occurrence of the one or more events through said I/O pins upon their detection; and

a workstation coupled to the logic board electronic design automation (EDA) software to provide said logic boards with said monitor and report requests.

17. The emulation system as set forth in claim 16, wherein the on-board data processing resources of each of the emulation IC comprise storage medium having stored therein programming instructions to operate the logic board to perform said local and corresponding retrieval, analysis, and reporting.

18. The emulation system as set forth in claim 17, wherein at least one of said emulation ICs of said logic boards comprises on-chip data processing resources to

cooperate and assist the on-board data processing resources of the logic board to perform said local and corresponding retrieval, analysis, and reporting.

19. An emulation system comprising:

a plurality of logic boards, each having a plurality of emulation integrated circuits (IC) including reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of partitions of an IC design, and on-board data processing resources to locally and correspondingly generate testing stimuli, and apply the generated stimuli to the emulated circuit elements of the partitions of the IC design being emulated, responsive to testing requests received through input/output (I/O) pins of the logic boards; and

a workstation coupled to the logic board, including electronic design automation (EDA) software to provide said logic boards with said testing requests.

20. The emulation system as set forth in claim 19, wherein the on-board data processing resources of each of the logic board comprise storage medium having stored therein programming instructions designed to operate the logic board to perform said local and corresponding generation and application of testing stimuli.

21. The emulation system as set forth in claim 19, wherein at least one of said emulation ICs of said logic boards comprises on-chip data processing resources to cooperate and assist the on-board data processing resources of the logic board to perform said local and corresponding generation and application of testing stimuli.

22. In an emulation system, a method of operation comprising:

locally and correspondingly retrieving state data of emulation state circuit elements of partitions of an IC design to be monitored from the emulation ICs, said partitions of the IC design being emulated by reconfigurable logic and interconnect resources of emulation ICs of logic boards of the emulation system;

locally and correspondingly analyzing the retrieved state data to detect one or more event; and

reporting the detected ones of said one or more events upon their detection.

23. The method as set forth in claim 22, wherein at least some of said performances of local and corresponding retrieval, analysis, and reporting are assisted by on-chip data processing resources of the emulation ICs of the logic boards.

24. In an emulation system, a method of operation comprising:

locally and correspondingly generating testing stimuli; and

locally and corresponding applying the generated testing stimuli to selected ones of the emulation circuit elements of partitions of an IC design being emulated.

25. The method as set forth in claim 24, wherein at least some of said performances of local and corresponding generation and application of testing stimuli are assisted by on-chip data processing resources of the emulation ICs of the logic boards.

26. An emulation integrated circuit (IC) comprising:

a plurality of reconfigurable logic and interconnect resources; and

on-chip data processing resources coupled to said reconfigurable logic and interconnect resources to locally retrieve state data of emulation state circuit elements of a partition of an IC design being emulated to monitor, analyze the retrieved state data of the emulation state circuit elements to detect occurrence of one or more events, and report on occurrence of said one or more events upon detecting their occurrence.

27. The emulation IC as set forth in claim 26 wherein said on-chip data processing resources comprises storage medium having stored therein programming instructions designed to perform said local analysis and reporting.

28. The emulation IC as set forth in claim 27, wherein said on-chip data processing resources further locally generate testing stimuli, and locally apply the generated testing stimuli to the partition of the IC design being emulated.

29. The emulation IC as set forth in claim 28, wherein said on-chip data processing resources comprises storage medium having stored therein programming instructions designed to perform said local generation and application of testing stimuli.

30. In an emulation integrated circuit (IC), a method of operation comprising:

locally retrieving on said emulation IC, using on-chip data processing resources, emulation state circuit elements of a partition of an IC design being emulated;

locally analyzing state data of the emulation state circuit elements, using on-chip data processing resources, to detect occurrence of one or more events; and

reporting on occurrence of said one or more events upon detecting their occurrence.

31. The emulation IC as set forth in claim 30, wherein the method further comprises

locally generating testing stimuli; and

locally applying the generated testing stimuli to an IC design being emulated.

32. An emulation integrated circuit (IC) comprising:

a plurality of reconfigurable logic and interconnect resources; and

on-chip data processing resources coupled to said reconfigurable logic and interconnect resources to locally generate testing stimuli, locally apply the generated testing stimuli to a partition of an IC design being emulated.

33. The emulation IC as set forth in claim 32, wherein said on-chip data processing resources comprises storage medium having stored therein programming instructions designed to perform said local generation and application of testing stimuli.

34. In an emulation integrated circuit (IC), a method of operation comprising:

locally generating on said emulation IC testing stimuli, using on-chip data processing resources; and

locally applying the testing stimuli, using said on-chip data processing resources, to emulation circuit elements of a partition of an IC design.